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EXAMINER	
RASHID, DAVID	
ART UNIT	PAPER NUMBER
2609	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/806,734	LOEW, ANDREAS	
	Examiner	Art Unit	
	David P. Rashid	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/23/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

All of the examiner's suggestions presented herein below have been assumed for examination purposes, unless otherwise noted.

Amendments

1. This office action is responsive to the preliminary claim and specification amendment received on March 23, 2004.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d) (Application # 10315442.6), which papers have been placed of record in the file.

Drawings

3. The drawings are objected to because of the following:

(i) The following is a quotation of 37 CFR 1.84(u):

View numbers must be proceeded by the abbreviation "FIG."

FIG. 1 – FIG. 6 view numbers contain lower-case characters – suggest changing all view numbers to upper-case character (ex. "Fig. 1" to "FIG. 1")

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet,

even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. 37 CFR 1.75(a) reads as follows:

> The specification must conclude with a claim particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention or discovery.

5. Claims 1- 9 are objected to because of the following informalities:

(i) It is unclear whether "pixels and/or subpixels" pertains to pixels AND subpixels, or pixels OR subpixels – suggest changing to "pixels or subpixels" for all the claims as will be assumed for examination purposes.

(ii) It is unclear whether "column-by-column and/or line-by-line" pertains to column-by-column AND line-by-line, or column-by-column OR line-by-line – suggest changing to "column-by-column or line-by-line" for all the claims as will be assumed for examination purposes.

(iii) Claim 9 is referring to the method as claimed in claim 8, but claim 8 is in fact a product ("scaling circuit") – suggest changing "The method as claimed in claim 8," to "The scaling circuit as claimed in claim 8,"

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. **Claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13,** and **14** are rejected under 35 U.S.C. 102(b) as being anticipated by Scott et al. (US 5,097,518 A).

Regarding **claim 1**, Scott et al. discloses a method for the arbitrary selectable scaling of input images represented by pixels or subpixels arranged line by line and column by column ("error diffusion pixel saving reduction scaling technique", column 5, line 12), wherein

selected pixels or subpixels which are intended for reproduction in the output images are determined in the input image (FIG. 4A, as the reproduction in the output images are determined in the input image by the direction of arrows under reference numerals 413, 417, 423, and 427 directed from source image 410 to reduced image 440),

the respective column-by-column or line-by-line distance of which being dimensioned in such a way as to achieve a rational scaling ratio of input image to output image at least over a range of a line or of a column by calculation of integer distances between successive selected pixels or subpixels of the input image with minimal variation between the distances ("As shown, source (original) image 410 is to be reduced by different scale factors in both the vertical and horizontal directions, e.g. illustratively 2.33 horizontally and 1.5 vertically, to yield reduced image 440. To achieve this reduction scaling, the source image is broken into pixel groups (blocks) of varying groupsizes both horizontally and vertically. The groupsize in the horizontal direction varies between the values 2 and 3 with the fractional variation occurring between horizontally successive pixel blocks averaging out to the fractional value 0.33. In particular, the horizontal groupsize periodically varies as given by the values 3, 2, 2, 3 and so on. At the same time, the groupsize also periodically varies in a vertical direction. To provide a vertical reduction factor of 1.5, the vertical groupsize varies between 1 and 2 with the fractional variation occurring between vertically successive pixel blocks averaging out to the fractional value 0.5.", column 14, line 4 in combination with FIG. 4A).

Regarding **claim 2**, Scott et al. discloses the method as claimed in claim 1, wherein the selected pixels or subpixels of the input image are used as support points which, in the output

image, are allocated a pixel or subpixel which is calculated or selected from a plurality of pixels or subpixels of the input image which precede or succeed the support point ("In particular, the horizontal groupsize periodically varies as given by the values 3, 2, 2, 3 and so on.", column 14, line 15. For this 2.33 horizontal scale factor example and the values 3, 2, 2, 3, 2, ... selected inherently produce support points in between specific pixels that border successive pixel blocks.

FIG. 4A depicts support points in between successive pixel blocks 411, 415, 421, and 425 composed of individual pixels. The support points are allocated a pixel that has been selected from a plurality of pixels of the input image, which precede or succeed the support point (in particular, the rightmost pixel of each successive pixel block in combination with the leftmost pixel of each proceeding successive pixel block if the horizontal/vertical scaling factor is not an integer, or the rightmost pixel itself of each successive pixel block if the horizontal/vertical scaling factor is an integer – both cases covered by Scott et al.).

Regarding **claim 3**, Scott et al. discloses the method as claimed in claim 2, wherein the preceding or succeeding pixels or subpixels of the input image in a range up to the respectively adjacent support point are used for the calculation ("With the pixel blocks defined in this manner, the individual pixels that form each block are then logically combined, through an "OR" operation, to yield a single corresponding pixel value that occupies a corresponding spatial location in the scaled image", column 14, line 25. As shown in FIG. 4A, each successive pixel block undergoes an "OR" operation which in effect is a calculation).

Regarding **claim 4**, Scott et al. discloses the method as claimed in claim 1,

wherein a value representing the scaling ratio is fed as addend to an adder (FIG. 7 "scaling sub-system", further reference numeral 720 "horizontal reduction system" as disclosed in detail in FIG. 8, and further reference numeral 1200 "groupsize error diffusion circuit" as disclosed in detail in FIG. 12. "Adder 1210 produces the sum of the fraction eight-bit groupsize value applied over leads 1203 and the current output appearing on leads 1255 of pass/ ½ FSR circuit 1250.", column 37, line 18).

wherein the addition of the addend is performed for each pixel or subpixel line by line or column by column and, in the case where a threshold value is exceeded, a support point is marked at the current pixel or subpixel (FIG. 12 groupsize error diffusion circuit takes the fractional groupsize value (ex. for groupsize value 2.33, the fractional groupsize value is 0.33) and adds to adder 1210. "Alternatively, generate a value of 0.33, the pattern "0, 1, 0, 0, 1, 0, . . . " is produced and so on for other fractional values.", column 37, line 13. It is inherent that the adder 1210 must use a constant number to produce the continuous patterns of 0s and 1s for any fractional value given (The change from "1" to "0" results from when this number is exceeded, or vice versa.), and this number can be considered a threshold value. Back to FIG. 8, the 0/1 from 1215 is added to integer groupsize value (820) to equate the current groupsize 825 that is fed into the next pixel position register 840. "Next pixel position register (NPPR) 840 is an eight-bit register that stores the position of the first pixel in the next group (block) to be processed, relative to bit zero of the current input word appearing on leads 715.", column 25, line 17. This first pixel in the next group (block) is considered a support point being marked.

wherein, after the marking of a support point, a value corresponding to the threshold value is subtracted from the content of the adder 1210 (The marking of a support point from the

next pixel position register 840 will automatically align with the pattern of 0s and 1s generated from adder 1210 to signal a new successive pixel block. Consider the example pattern "0, 1, 0, 0, 1, 0..." generated from the fraction groupsize value 0.33 (groupsize value 2.33). The change from "1" to "0" is a subtraction due to the threshold value within the adder 1210. This change will eventually occur after the marking of a support point in the NPPR 840.).

Regarding **claims 5**, Scott et al. discloses the method as claimed in claim 4, wherein the exceeding of the threshold value is signaled by the state change of a selected bit in a binary adder (refer to the references cited in claim 4 - the change from "1" to "0" in particular.).

Regarding **claim 6**, Scott et al. discloses the method as claimed in claim 5, wherein the subtraction of the threshold value is performed by continued addition and disregarding of the overflow of the binary adder ("As discussed above, circuit 1200, based upon the fractional groupsize value, generates an evenly distributed pre-defined pattern of successive "1's" and "0's" on lead 1215 which averages out to this fractional value. Each successive value in this pattern is generated at each successive clock pulse the NEXT VALUE and Clock Enable inputs to the groupsize generator.", column 37, line 4.). Each successive value in the pattern generated at each successive clock pulse is stored as the NEXT VALUE input to the groupsize generator and because of this, the binary adder overflow is not considered.

Regarding **claims 7** and **9**, Scott et al. discloses the method wherein successive lines or columns are processed with an offset by whole pixels or subpixels (FIG. 4A depicts offsets by

whole pixels for both successive lines or columns of the output image 440 (as well as input image 410). For example, successive output columns with uppermost pixels 441, 442, 443, 444, ... are processed with an offset by whole pixels. Output column with uppermost pixel 442 was processed with an offset of 3 columns from the left edge of the input image 410, and calculations start at input column with uppermost pixel 415_1. Output column with uppermost pixel 443 was processed with an offset of 5 columns from the left edge of the input image 410, and calculations start at input column with uppermost pixel 421_1.).

Regarding **claim 8**, Scott et al. discloses a scaling circuit for the arbitrarily selectable scaling of images represented by pixels or subpixels arranged line by line and column by column ("Separate scaling circuits are used not only for both reduction and enlargement scaling but also in each scaling direction, i.e. the horizontal and vertical directions.", column 22, line 52.), having

a microprocessor ("Central processing unit 220, which can contain any one of many well known microprocessors, controls the operation of the workstation.", column 10, line 7.),

a program memory and a main memory ("Memory 215 is formed of read only (ROM) memory 216 that stores a control program, such as a boot strap loader, and random access (RAM) memory 217 that is used as a temporary program and data store during execution of the control program.", column 10, line 26.), and

also input means for scaling ratios ("Within scaler 720, the current groupsize is generated through groupsize error diffusion circuit 1200 and adder 820 shown in FIG. 8.", column 24, line 25.),

wherein a method as claimed in claim 1 is executable in program-controlled fashion ("Specifically, the processor, operating under stored program control...", column 10, line 15.).

Claim 8 is also rejected under 102(b) as being anticipated by the Intel 80386 computer first produced in 1986. The Intel 80386 computer has a microprocessor, a program memory and a main memory, and input means for scaling ratios (intended usage if one decides to use the keyboard or mouse), wherein a method as claimed in claim 1 is executable (intended usage if one decides to program into the Intel 80386 computer).

Regarding **claim 10**, Scott et al. discloses a scaling circuit for the arbitrarily selectable scaling of images represented by pixels or subpixels arranged line by line and column by column,

having adders, in which values representing a scaling ratio can be added for each pixel or subpixel in lines or columns (adders, reference numerals 820, 1210, etc), respectively,

input means for scaling ratios ("Within scaler 720, the current groupsize is generated through groupsize error diffusion circuit 1200 and adder 820 shown in FIG. 8.", column 24, line 25.),

a comparator for the lines or columns, respectively, which signals the exceeding of a threshold value by the addition (),

a first multiplexer, by means of which the pixels or subpixels of a line can be allocated values (It is known to one ordinary skilled in the art that a multiplexer is a device that encodes or

multiplexes information from two or more data sources into a single channel. FIG. 8 pass/zero circuit reference numeral 850 is a multiplexer for the horizontal reduction scaler.),

a second multiplexer, by means of which the pixels or subpixels of a column can be allocated values (FIG. 9 shows a series of gates from reference numeral 953 through 967 to produce single line 735.) and

a memory for storing the values for pixels or subpixels for lines or columns (The NPPR is one of the many circuits for storing the values for pixels for lines or columns. "Next pixel position register (NPPR) 840 is an eight-bit register that stores the position of the first pixel in the next group (block) to be processed, relative to bit zero of the current input word appearing on leads 715.", column 25, line 17.).

Regarding **claim 11**, Scott et al. discloses the scaling circuit as claimed in claim 10, wherein means are provided for storing selected bit positions of the adder (groupsize error diffusion circuit within FIG. 12 in combination with "Inasmuch as an eight-bit register is used to implement register 1240, the largest (full scale) value that can be store within this register is "256" and hence the fixed value equals "128".", column 37, line 52.) and

means for comparing successive contents at the selected bit positions, wherein an exceeding of the threshold value is identifiable on the basis of a state change of successive contents at the selected bit positions of the adder ("As discussed above, circuit 1200, based upon the fractional groupsize value, generates an evenly distributed pre-defined pattern of successive "1's" and "0's" on lead 1215 which averages out to this fractional value. Each successive value in

this pattern is generated at each successive clock pulse the NEXT VALUE and Clock Enable inputs to the groupsize generator.", column 37, line 4.).

Regarding **claims 12, 13,** and **14**, Scott et al. discloses a film scanner with a drive for a control monitor ("Given the instructions received from the host computer, the scanner node controls the film library to fetch and load a specified roll of microfilm into a microfilm reader contained within the library and thereafter advance the roll to a specified frame. The scanner node then electronically scans and digitizes a gray scale microfilm image present at the specified frame into a bit-mapped bi-tonal image typically at a resolution of 300-400 dots/inch (approximately 118-157 dots/centimeter--cm), compresses the resulting bit-mapped bi-tonal image, and finally applies the compressed image as a packet with a suitable header (well known and not shown) onto local area network 15.", column 9, line 2.).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David P. Rashid whose telephone number is (571) 270-1578. The examiner can normally be reached on 7:30 - 17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Werner can be reached on (571) 272-7401. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DPR

David P Rashid
Examiner
Art Unit 2112

BRIAN WERNER
SUPERVISORY PATENT EXAMINER